Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 35955	SERIAL NO. 10/627,479
INFORMATION DISCLOSURE CITATION BY APPLICANT *(USE SEVERAL SHEETS IF NECESSARY)*	APPLICANT: **Kazushi Higashi et al.**	
Page 1 of 1	FILING DATE: **July 25, 2003**	GROUP ART UNIT: ~~4217~~ 3729

U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Date	Name	Class	Subclass	Filing Date
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						

FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Class	Subclass	Translation
CJA	I	3-241755	10/1991	JP			Eng. abstract & Partial Trans. Attached
	J						

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)*

CJA	K	"Development of chip-on-chip bonding process at a room temperature (with copper, a bumpless bonding is also possible)", Semiconductor Sangyo Newspaper, June 12, 2002, pg. 9, Sangyo Times Inc., Tokyo, Japan.
CJA	L	"Development of chip-on-chip bonding process at a room temperature by a superbonder", Electronic Materials, July 1, 2002, pp. 8-9, Vol. 41 No. 7, Kogyo Chosakai Publishing Co., Ltd., Tokyo, Japan.
CJA	M	"Ultrasonic Flip Chip Bonding Technology for LSI Chip with High Pin Counts" by Kajiwara et al., from Proceedings of the 7th Symposium on Microjoining and Assembly Technology in Electronics, February 1, 2001, pp. 16166, Japan Welding Society, Tokyo, Japan.
	N	

Examiner: C. J. Arbes	Date Considered 6/10/05

*Examiner: Initial if reference considered, regardless of whether citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.